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CONFIRMATION NO. 3056

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APPLICANTS Satoshi Sakai, Yokohama, JAPAN; Satoshi Yamamoto, Takarazuka, JAPAN; Atsushi Hiraiwa, Higashimurayama, JAPAN; Ryoichi Furukawa, Ome, JAPAN;				
** CONTINUING DATA ***** This application is a 371 of PCT/JP02/08284 08/15/2002				
** FOREIGN APPLICATIONS *****				
Foreign Priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after met Allowance Verified and Acknowledged		STATE OR COUNTRY JAPAN	SHEETS DRAWING 45	TOTAL CLAIMS 19
Examiner's Signature _____ Initials _____		INDEPENDENT CLAIMS 2		
ADDRESS Mattingly Stanger & Malur 1800 Diagonal Road Suite 370 Alexandria ,VA 22314				
TITLE Semiconductor integrated circuit device and method for fabricating the same				
FILING FEE RECEIVED 1030	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit	